

Notice of References Cited		Application/Control No.	Applicant(s)/Patent Under Reexamination	
		10/712,288	CHAVES FILHO, ELISEU M.	
Examiner		Art Unit		Page 1 of 1
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	J	US-			
	K	US-			
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	M	US-			

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	V	Lee et al, Design and Implementation of the MorphoSys Reconfigurable Computing Processor, Journal of VLSI Signal Processing Systems, pages 1-38, 2000.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.